WHAT IS CLAIMED IS:

1. An integrated circuit comprising an array of DRAM cells, each DRAM cell comprising:

a first transistor having a gate coupled to a read word line and a drain coupled to a read bit line;

a second transistor coupled in series between the first transistor and a power supply voltage; and

a third transistor coupled between the gate of the second transistor and a write bit line, a gate of the third transistor being coupled to a write word line,

wherein the write word line is not directly connected to the read word line.

2. The integrated circuit according to claim 1 wherein the integrated circuit is a field programmable gate array, and the gate of the second transistor is coupled to a pass gate in the field programmable gate array.

3. The integrated circuit according to claim 2 wherein the pass gate is a programmable routing connector that couples interconnect lines on the field programmable gate array.

4. The integrated circuit according to claim 2 wherein the pass gate is used to configure logic performed by logic circuitry on the field programmable gate array.

5. The integrated circuit according to claim 1 further comprising:

a capacitor coupled to a gate of the second transistor.

6. The integrated circuit according to claim 5 wherein the capacitor is a planar capacitor or a trench capacitor.

7. The integrated circuit according to claim 5 wherein the capacitor is a quasi-static DRAM capacitor fabricated with nano-crystal oxide.

8. The integrated circuit according to claim 1 further comprising:

a CMOS inverter having an input coupled to the gate of the second transistor,

wherein the integrated circuit is a programmable integrated circuit, and an output of the CMOS inverter drives a pass gate that programmably couples interconnect lines on the programmable integrated circuit.

9. The integrated circuit according to claim 8 wherein the third transistor is a p-channel field effect transistor, and the input of the CMOS inverter is not directly connected to an N-type doped semiconductor region.

10. The integrated circuit according to claim 1 further comprising:

a sense amplifier having an input coupled to the read bit line;

a multiplexer having a first input coupled to an output of the sense amplifier; and

a driver coupled between an output of the multiplexer and the write bit line.

11. The integrated circuit according to claim 10 further comprising:

a data shift register coupled to a second input of the multiplexer;

an error detection circuit coupled to an output of the data shift register, the error detection circuit performing error detection on data stored in the DRAM cells.

12. An integrated circuit comprising an array of DRAM cells, each DRAM cell comprising:

a first transistor having a gate coupled to a read word line and a drain coupled to a read bit line;

an inverter having an output coupled to a source of the first transistor; and

a second transistor coupled between an input of the inverter and a write bit line, a gate of the second transistor being coupled to a write word line.

13. The integrated circuit as defined in claim 12 wherein the integrated circuit is a programmable integrated circuit and the output of the inverter is coupled to a pass gate.

14. The integrated circuit as defined in claim 12 wherein the second transistor is a p-channel transistor, and the input of the inverter is not directly connected to an N-type doped semiconductor region.

15. The integrated circuit as defined in claim 12 further comprising a capacitor coupled to the input of the inverter.

16. The integrated circuit as defined in claim 15 wherein the capacitor is a planar capacitor or a trench capacitor.

17. The integrated circuit as defined in claim 15 wherein the capacitor is a quasi-static DRAM capacitor fabricated with nano-crystal oxide.

18. The integrated circuit as defined in claim 12 further comprising:
a sense amplifier having an input coupled to the read bit line; and
a multiplexer coupled between an output of the sense amplifier and the write bit line.

19. A method for storing data in and accessing data from a DRAM cell, the method comprising:
applying a first voltage on a write word line to turn on a first transistor;
applying a second voltage on a write bit line coupled to a drain of the first transistor to store charge at a gate of a second transistor;
applying a third voltage on the write word line to turn off the first transistor;
applying a fourth voltage on a read word line to turn on a third transistor, wherein the second transistor is coupled in series with third transistor; and
sensing a fifth voltage on a read bit line coupled to a drain of the third transistor, the second and third transistors conducting current between the read bit line and a supply voltage if the charge stored at the gate of the second transistor is a first logic state,
wherein the write word line is not directly connected to the read word line.

20. The method according to claim 19 wherein a capacitor is coupled to the gate of the second transistor to store the charge.

21. The method according to claim 20 wherein a gate of a fifth pass gate transistor is coupled to the capacitor and the gate of the second transistor, the pass gate coupling two segments of programmable routing wires.

22. The method according to claim 19 wherein an input of an inverter is coupled to the gate of the second transistor.

23. The method according to claim 22 wherein the first transistor is a p-channel transistor.

24. The method according to claim 19 wherein sensing the fifth voltage on the read bit line further comprises:

amplifying the fifth voltage using a sense amplifier; and

driving an output signal of the sense amplifier to the write bit line to refresh the charge stored at gate of the second transistor.

25. The method according to claim 19 further comprising:

detecting errors in the data stored in the DRAM cell.

26. A method for storing data in and accessing data from a DRAM cell, the method comprising:

applying a first voltage on a write word line to turn on a first transistor;

applying a second voltage on a write bit line coupled to a drain of the first transistor to store charge at an input of an inverter;

applying a third voltage on the write word line to turn off the first transistor;

applying a fourth voltage on a read word line to turn on a second transistor, wherein the second transistor is coupled to an output of the inverter; and

sensing a fifth voltage on a read bit line coupled to a drain of the second transistor, the second transistor conducting current between the read bit line and the output of the inverter if the charge stored at the input of the inverter is a first logic state.

27. The method according to claim 26 wherein the first transistor is a p-channel transistor and the second transistor is an n-channel transistor.

28. The method according to claim 26 further comprising:

coupling the output of the inverter to a pass gate,

wherein the DRAM cell is part of a memory array of DRAM cells, and the memory array and the pass gate are part of a programmable integrated circuit.

29. The method according to claim 26 wherein sensing the fifth voltage on the read bit line further comprises:

amplifying the fifth voltage using a sense amplifier;

selecting an output signal of the sense amplifier using a multiplexer; and

driving an output signal of the multiplexer to the write bit line to refresh the charge stored at the input of the inverter.

30. The method according to claim 29 further comprising:

detecting errors in the data stored in the DRAM cell.

31. A method for verifying data stored in a row of DRAM cells, the method comprising:

applying a first voltage on a read word line to turn on first transistors in the row of DRAM cells;

sensing second voltages on read bit lines coupled to drains of the first transistors using sense amplifiers, each first transistor conducting current between the read bit line and a supply voltage if the charge stored in the DRAM cell is a first logic state;

receiving output signals of the sense amplifiers in shift registers;

shifting the output signals through the shift registers to an error detection circuit; and

detecting errors in the data using the error detection circuit.

32. The method as defined in claim 31 wherein each of the DRAM cells further comprises:

a second transistor coupled in series between the first transistor and the supply voltage; and

a third transistor coupled between a gate of the second transistor and a write bit line, a gate of the third transistor being coupled to a write word line.

33. The method as defined in claim 31 wherein each of the DRAM cells further comprises:

an inverter having an output coupled to a source of the first transistor; and

a second transistor coupled between an input of the inverter and a write bit line, a gate of the second transistor being coupled to a write word line.

34. A method for refreshing and verifying data stored in an array of DRAM cells, the method comprising:

applying a first voltage on a read word line to turn on first transistors in a row of DRAM cells;

amplifying second voltages on read bit lines coupled to drains of the first transistors using sense amplifiers, wherein each first transistor conducts current between the read bit line and a supply voltage if the charge stored in the DRAM cell is a first logic state;

applying a third voltage on a write word line to turn on second transistors that are each coupled to a node storing charge representing a bit of data;

driving output signals of the sense amplifiers to write bit lines to refresh the charge stored in the nodes; and

detecting errors in the data stored in the row of DRAM cells using the output signals of the sense amplifiers,

wherein the error detection and the refresh of the charge stored in the nodes are performed concurrently.

35. The method as defined in claim 34 wherein each of the DRAM cells further comprises:

a third transistor coupled in series between the first transistor and the supply voltage,

wherein each second transistor is coupled between a gate of the third transistor and one of the write bit lines.

36. The method as defined in claim 34 wherein each of the DRAM cells further comprises:

an inverter having an output coupled to a source of the first transistor,

wherein one of the second transistors is coupled between an input of the inverter and a write bit line.

37. A method for refreshing data stored in an array of DRAM cells in an integrated circuit, the method comprising:

applying a voltage on a write word line to turn on write transistors in each DRAM cell within a row of DRAM cells;

shifting refresh data signals into data shift registers from a source external to the integrated circuit;

selecting the refresh data signals stored in the data shift registers using multiplexers; and

driving the refresh data signals to write bit lines to refresh charge signals stored in the row of DRAM cells, wherein each of the write transistors is coupled to one of the write bit lines.